IN THE SPECIFICATION

Please amend the paragraph beginning on page 7, line 10, as follows:

For some embodiments, providing the local digital information may include dynamically receiving video data associated with each display element. However, receiving the video data, in one embodiment, includes programmably ~~programmablly~~ receiving at least one pixel value for each display element. The digital information may be programmably ~~programmbally~~ stored in at least one register associated with each display element. Then, for each display element, a duration of illumination, i.e., an "ON" time within the refresh period may be caused based on the length of the first pulse interval of the modulated signal.

Please amend the paragraph beginning on page 13, line 11, as follows:

Forced delays may be introduced in some embodiments to generate an adjusted PWM waveform, for example, having a time period indicated as T_{pwm} 165. In particular, a first force "ON" time, T_{f1}, 170a, and a second force "OFF" ~~"ON"~~ time, T_{f0}, 170b, may be introduced in one embodiment. Adding additional delay between the steps 2 and 3 creates the first force "ON" time, T_{f1}. Adding additional delay between the steps 3 and 4 creates the second force "OFF" time, T_{f0}. Although adding these times can bound the minimum and maximum portion of the first and second refresh time periods, i.e., T_r 150a and 150b, that is spent within the PWM waveform during the "ON" state, however, a new PWM waveform with a single transition may still be generated accordingly.

Please amend the paragraph beginning on page 15, line 13, as follows:

Each register 85 (Figure 2) of the plurality of registers 85(1) through 85(N) may dynamically receive video data associated with a different display element to cause the "ON" time within the refresh period based on the corresponding linearly pulse width modulated waveform at block 180. Corresponding digital information including video data having a corresponding pixel value may be programmably ~~programmbally~~ received at each display element. More specifically, each register 85 of the plurality of registers 85(1) through 85(N) may store the corresponding pixel value 90 of the plurality of pixel values 90(1) through 90(N) at block 182.